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EXAMINER	
NGUYEN, VAN THU T	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 03/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/626,775	KANG, HEE BOK
	Examiner	Art Unit
	VanThu Nguyen	2824

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02/01/2005 - Amendment*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,19 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,19 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/05/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

1. Acknowledgement is made for Amendment filed on February 1, 2005.

2. Claims 1-10, 19-20 are still pending.

3. Claims 11-18 are cancelled.

Response to Arguments

4. Regarding claims 1 and 19, Applicant's arguments filed February 1, 2005 have been fully considered but they are not persuasive.

5. Regarding claims 1-2, 19-20, Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection under U.S. Patent No. 6, 707,757 by Roohparvar.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claims 2-8 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention as following:

Specification does not disclose "the register command processor configured to ... control the plurality of registers **to store** the control data according to the identified mode" as in claim 2, line 6

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1-2, 19-20 are rejected under 35 U.S.C. 102(e) as being anticipated by **Keays** (U.S. Patent No. 6,614,695) or **Roohparvar** (U.S. Patent No. 6, 707,757).

Keays discloses (in FIG. 1):

Regarding claim 1, a memory device (100) capable of controlling a characteristic parameter (skip over a row), comprising:

a register controller (130) for storing control data (such as track/flag if associated row in associated block being erased or unverified); and

a parameter controller (108) configured to output a signal having a characteristic parameter (skip over a row) depending on the control data outputted from the register controller (such as unverified signal), wherein the register controller is nonvolatile (see column 6, lines 3-5).

(See column 6, line 64 to column 7, line 11)

Regarding claim 19, it is rejected under U.S.C. 102(e) since it recited similar limitations as in claim 1.

Roohparvar discloses:

Regarding claim 1, a memory device (100, see FIG. 8) capable of controlling a characteristic parameter (either skip or implement an operation), comprising:

a register controller (Flow Control Register 110 in FIG. 8, Test Mode Detector/Decoder 102 in FIG. 8 and its detail circuit diagram in FIG. 7, AND/OR gate 500 in FIG. 10) for storing control data (as shown in FIGS. 9-10); and

a parameter controller (State Machine 20, see FIG. 8) configured to output a signal having a characteristic parameter (either skip or implement an operations) depending on the control data outputted from the register controller, wherein the register controller is nonvolatile (see column 13, lines 7-13).

Regarding claim 2, the register controller comprises:

a register array comprising a plurality of registers for storing the control data (see FIGS. 9-10);

a register command processor (Test Mode Detector/Decoder 102 in FIG. 8 and its detail circuit diagram in FIG. 7, Flow Con. Circuitry 112 in FIG. 8, and AND/OR gates 500 in FIG. 10) configured to receive a plurality of signals (/CE, /WE, Address Pad, I/O Pads, see FIG. 7), to identify a mode as a program mode or a read mode (one of the output 504 in FIG. 10) by decoding the plurality of signals ((/CE, /WE, Address Pad, I/O Pads are decoded as shown in FIG. 7 with output signal 502, which input into AND/OR gates 500 as shown in FIG. 10), and individually control the plurality of registers to store the control data according to the identified mode (via Flow Con. Circuitry 112 in FIG. 8, also see column 13, lines 9-12), wherein the plurality of registers are nonvolatile.

Regarding claim 19, an integrated circuit device (100, see FIG. 8) capable of receiving an input signal (one of /CE, /WE, Address Pad A10, I/O Pads, as shown in FIG. 7) and generating an output signal (output of the X Decoder/Block Erase Control 14, see FIG. 8) having signal performance characteristics (either skip or implement an operation), comprising:

signal performance characteristic controller (Test Mode Detector/Decoder 102, Flow Control Register 110, Flow Con. Circuitry 112, State Machine 20, X Decoder/Block Erase Control 14 as shown in FIG. 8) to control one or more of the signal performance characteristics (either skip or implement an operation) of the output signal.

Regarding claim 20, the signal performance characteristic controller comprising:

a register controller (Test Mode Detector/Decoder 102 shown in FIG. 8 and it detail circuitry shown in FIG. 7) configured to provide a plurality of control signals (Test Mode Signals, see FIG. 7);

a plurality of nonvolatile registers (Flow Control Register 110 as shown in FIG. 8 and its detail circuitry shown in FIG. 10) each coupled to the register controller to receive one of the plurality of control signals and for storing and outputting a control data signal (output data from registers 1-10 as shown in FIG. 10); and

a plurality of AND and OR gates configured to receive control data signal from at least one of the plurality of nonvolatile registers and provide a common output (output from State Machine 20 as shown in FIG. 8); it is inherent that AND

and OR gates comprising transistors having source coupled to a voltage source, gate coupled to control data signal from nonvolatile registers, and drains providing outputs)

wherein the common output (output from State Machine 20 as shown in FIG. 8) controls the signal performance characteristic (either skip or implement an operation) of the output signal from the integrated circuit device.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Keays/Roohparvar and Komatsuzaki (PGPUB. 2004/0047172).

Keays/Roohparvar discloses, as applied in prior rejection of claim 1, all claimed subject matter except further limitations as in claims 9-10, Keays disclose the memory device having flash memory arrays, and Roohparvar disclose the memory device having non-volatile memory arrays.

Komatsuzaki discloses, in FIG. 12, a ferroelectric memory device having ferroelectric memory arrays comprising:

a plurality of unit cells;

a plurality of switches (for each unit cells); and

bit lines comprising sub bit lines connected to the plurality of unit cells and a main bit line connected to the plurality of sub bit lines via the plurality of switches,

wherein the plurality of switches is configured so that when a predetermined unit cell of the plurality of unit cells is accessed, only a switch for connecting a particular one of the plurality of sub bit lines connecting the predetermined unit cell to the main bit line is turned on, and other switches for connecting the rest of the plurality of sub bit lines to the main bit line are all turned off (corresponding to selected word line and sub bit line).

Since Keays/Roohparvar and Komatsuzaki are both from the same field of endeavor, the purpose disclosed by Komatsuzaki would have been recognized in the pertinent art of Keays/Roohparvar.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to use FeRAM because FeRAM is also an applicable non-volatile memory type, which is for controlled.

Allowable Subject Matter

12. Claims 3-8 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 1st paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VanThu Nguyen whose telephone number is (571) 272-1881. The examiner can normally be reached on Monday-Friday, 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

March 18, 2005

VanThu Nguyen
Primary Examiner
Art Unit 2824